Q.P. Code: 16CS510 R16

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations July-2022

COMPUTER ORGANIZATION

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Write in detail about Data Transfer Instructions	L2	5M
	b	Write in detail about Program Control Instructions	L2	7M
		OR		
2	a	Explain in detail about Instruction Cycle with neat sketch	L2	6M
	b	Write about Memory-Reference-Instruction	L2	6M

UNIT-II

3		Draw the H/W Flowchart and H/W Algorithm for Add/Sub of SMR with an example.	L2	12M
		OR		
4		Show the step by step signed-operand multiplication process using Booth algorithm when (-9) and (-13) are multiplied. Assume 5-bit registers to hold signed numbers and (-9) to be the multiplicand.	L3	12M

UNIT-III

5	a	Show that the block diagram of the hardware that implements the following register transfer statement P: R2←R1.	L3	6M
	b	Explain about the way of constructing a 4 line common bus system using multiplexers with a neat diagram.	L2	6M
		OR		
6		Explain in details about all three types of Shift Register Operations.	L2	12M

UNIT-IV

7	a	Explain about Memory Hierarchy.	L2	7M
	b	Explain about Memory Management Requirements.	L2	5M
		OR		
8	a	List out some differences between RAM & ROM.	L2	6M
	b	List out some differences between SRAM & DRAM.	L2	6M

UNIT-V

9	a	Explain about Parallel Processing and its Types.	L2	7M
	b	Explain the concept of Pipelining with clear example with neat sketch.	L2	5M
		OR		
10		Explain about Inter Process Communication & Synchronization in detail.	L2	12M

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